INTERNAL AND EXTERNAL CLOCK SYNCHRONIZATION IN A POWER LINE NETWORK

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Abstract

The nontrivial problem of distributing time in communication networks is not only limited to the Internet world, where this is nowadays solved by NTP. As the digital divide gap has not only to be closed between the last mile to the end user's PC and the nearest service point, also other systems like substation automation or energy meter management can benefit from a global notion of time as a service. As the usual high-performance Ethernet is, for the simple cost reasons of the cabling, not the most promising candidate to reach such nodes, other technologies such as power lines have to be investigated. This paper proposes a hierarchical clock synchronization scheme for power line networks.

INTRODUCTION

One very promising approach for low-cost clock distribution in large-scale systems is the usage of power line communication (PLC) systems. For this type of communication medium, clock synchronization is a crucial issue, not only because the PLC network itself requires synchronized clocks for maintaining time-sliced communication, but also for backbone networks and access points to establish a coordinated, fault-tolerant system-wide time base. This is needed in order to ensure fast log-on and log-off of nodes travelling from one access point to another. The problem of nodes and node groups disappearing on one side of the network and reappearing at different points, most likely at a different hierarchy as well, is caused by the usual way of energy suppliers switch whole net-groups from one transformer station to another, thus changing the logical hierarchy of the PLC network significantly. This paper will present an approach to synchronize clocks in such a system using the emerging standard IEEE 1588 **[1]**. In the lower levels of the hierarchical system, attention has to be paid to the special properties of the PLC network with respect to varying network topologies, short message length, and the like. To tackle this, a methodology using the IEEE 1588 format and protocol stack is presented.

The proposed system is implemented within the EU-founded REMPLI (Real-time Energy Management of Power Lines and Internet) project **[2]**. The goal of REMPLI is to establish a communication infrastructure using the existing wiring of power lines in order to manage energy consumption more efficiently and inexpensively than today. For example, remote meter reading is done in REMPLI by attaching up to four energy meters to every REMPLI node. Using this communication infrastructure, metering data can be retrieved without sending a physical person to read-out the meter. Moreover, if clocks between the nodes are synchronized, additional features like theft detection and energy flow analysis can be done. This detection of energy theft is done by advising all nodes in advance to record their meter values at a certain, predefined point in time **[3]**. Thus, by comparing the sum of all meters to the overall power supplied to the network, manipulations and energy thefts can be detected and localized easily.

This paper presents the implementation of such a large-scale system with cascaded clocks, reaching an overall accuracy of 200 µs in an area of several kilometers. The solution for a large-scale clock synchronization has to tackle the accuracy at steady-state, as well as the impact of transient effects like a coordinated, fast, and jitter-free power-up of the whole network.

PROPOSED SOLUTION

The fact that time is, in general, distributed hierarchically and, analyzing the margin conditions of power line networks, it seems clear one should divide the different tasks within the network structure into three stages:

- A fault-tolerant backbone network, setting up the reference time. Nodes in this network are equipped with a GPS receiver, MCXO, OCXO, or even an atomic clock.

- An underlying access network, where the access points reside. The main purpose of this network is high-speed data transport from and to the access points, providing synchronized clocks for:

- the PLC network, where the nodes, which communicate with the access points are finally synchronized over bridges or additional repeater levels.

The second network can be, depending on the application needs, combined with the first, by shrinking it and providing the reference time from a single node, which also functions as an embedded access point.

The considerations of the previous section lead to a three-level architecture consisting of hierarchically structured synchronization subnets (SSNs) like in NTP. The reference time is broadcasted by GPS satellites and atomic clocks, respectively. The GPS receivers, which are considered as reference clocks, are coupled directly to the nodes of the master group, which can be interpreted as a fully democratic subnet where each member of the group talks to all others. This approach has the advantage that a failure of a single master has hardly any influence on the slaves associated, except that the overall accuracy of the master group is reduced. Within the master group the democratic SynUTC **[5]** protocol is used to synchronize the participating nodes. Nevertheless, other democratic and fault tolerant approaches can be used as well.

The master group nodes determine a fault-tolerant average value of the current time and pass it on to all IEEE 1588 slaves. The transmission takes place via a so-called master group speaker, represented by the switches in Figure 1. This speaker and the switches for the cross-linking of the master group must also offer the possibility for redundancy on the physical and on the protocol layer. In the case of the REMPLI project, the boarder to the slaves is build by the access point, which also translates between Ethernet and power line protocol.

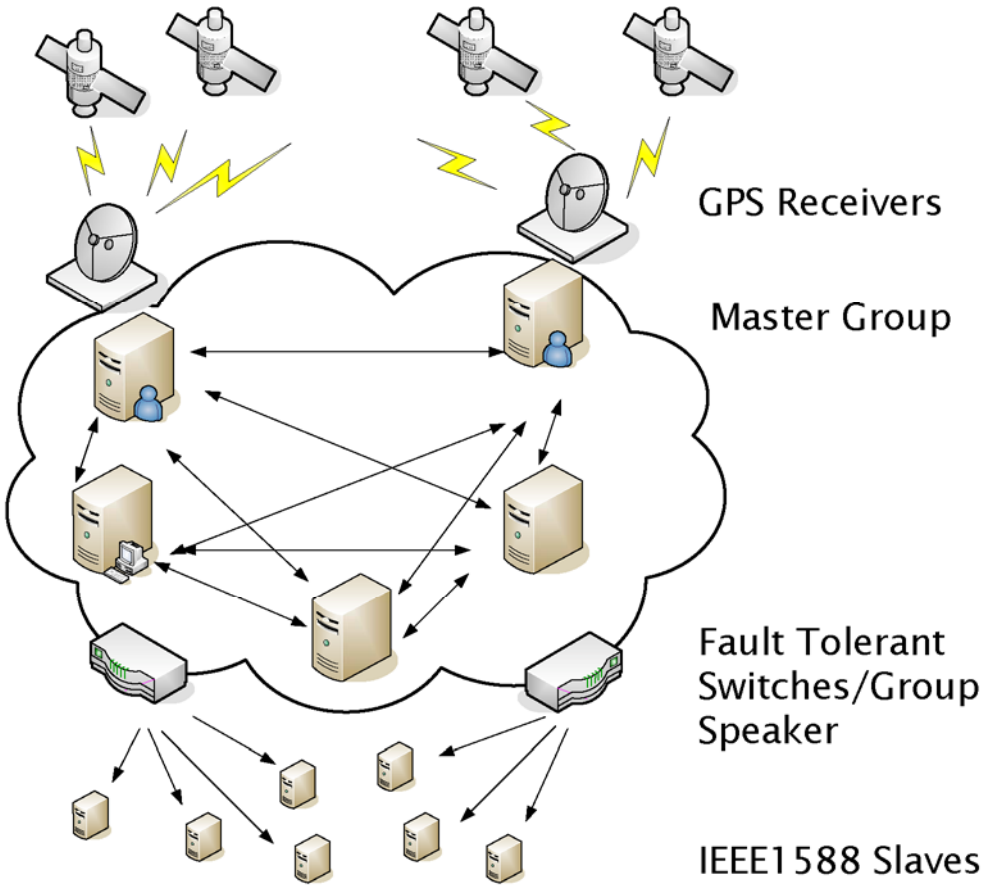

Figure 1. Master group concept.

The group speaker communicates with a set of standard IEEE 1588 (version 2002) slaves, which ensures low traffic volume (compared to the reference clock interconnection) even for high numbers of slaves. The associated master for each node is the speaker of the super-ordinate group, which acts transparently like an IEEE 1588 master and passes the ensemble time from the group downward. The very heart of this approach is to enhance IEEE 1588 networks with this transparently integrable master group to a hybrid architecture in order to increase stability and fault tolerance.

SETTING UP THE REFERENCE TIME

As already mentioned, the reference time is kept in a reliable backbone network, which consists of Ethernet nodes, each enabled to keep an accurate time source. For cost reasons, this is done via GPS receivers, which are coupled directly to the nodes. This approach has the advantage that a failure of a single master has hardly any influence on the slaves associated, except that they have to switch to a new (but synchronous) time source.

ACCESS NETWORK

The access network in the REMPLI project is an Ethernet network, where clocks are synchronized using the IEEE 1588 standard for clock synchronization. To gain a precision below 5 µs, adapted Ethernet hardware is also required, capable of timestamping arriving packets and cancelling out communication

delays. This specialized hardware needs and implementation are described in **[3]** and are integrated into the central embedded processor (Hyperstone hyNet 32XS) used in the mentioned project.

POWER LINE NETWORK

On the evaluation boards, the PLC physical layer communication is done using a separate ASIC, with a signal processing unit for mixing, filtering, up- and sub-sampling as well as synchronization detection. A finite state machine (FSM) controls all states for transmitting and receiving data. This FSM can be configured from an integrated DSP and is fully predictable, which allows easy verification of all states. In order to detect synchronization events properly, the complete module performs an energy-normalized correlation of complex synchronization sequences on the equivalent complex base band. Further, it generates, by the use of a threshold, a frame clock event for connected onboard modules. As a synchronization sequence, a complex Barker sequence or other complex synchronization sequences especially designed for single-frequency networks **[4]** can be used.

One of the obviously most important differences between the power line communication technology used in REMPLI and high-bandwidth, highly reliable communication networks like Ethernet is the lack of bandwidth. Nevertheless, the advantage of the proprietary character of the power line eases the use of lower-level network services, such as a relatively jitter-free frame clock which all telegrams over the power line are aligned to.

Another problem is that the analyzed system is in general not capable of providing symmetric communication channels in terms of latency. As the concept of PTP relies on a symmetric channel, a non-negligible error would be made if PTP is used over native power line. This means that asymmetry needs to be compensated, which can be done by predefined correction values. As a second issue, as transportation costs from a master in a power line is disproportionally higher than in the other direction, the implementation simulates the IEEE 1588 **delay_request** and **delay_response** messages and prohibit the sending and receiving of these messages by generating replies on the slave nodes with predefined answer delays in a so-called *adaptation layer*. Figure 2 shows the integration of this adaptation layer into the REMPLI node structure.

Also the IEEE 1588 **follow_up** messages, which contain the exact time of a sent message, have to be emulated by the adaptation layer. As in this case, the exact arrival and sent time of messages is defined by the frame clock; the **follow_up** messages can be generated within the adaptation layer. The fact that all other messages are aligned to the system-wide frame clock as well is used to have the adaptation layer also use the occurrence of these messages for generation of synchronization packets. The drawback, that no absolute time is sent with these messages, can be tackled with a prediction function of scheduled frame-clock events, which is defined via the communication speed. Finally, also the arrival of a real sync packet is used to adjust the prediction algorithm. Figure 3 shows the translation scheme of the adaptation layer.

Finally, the node management concept has to be mentioned as well. As IEEE 1588 uses so-called management messages to control certain properties of the node itself, these messages have to be fed to the node as well. The advantage of the adaptation layer is that a regular IEEE 1588 stack can be used with the same timestamp format regardless of the underlying communication media. For sure, the node configuration has to be set up in a way that the logical IEEE 1588 topology is the same as the PLC topology, which means that the PLC master node is equivalent with the IEEE 1588 master node.

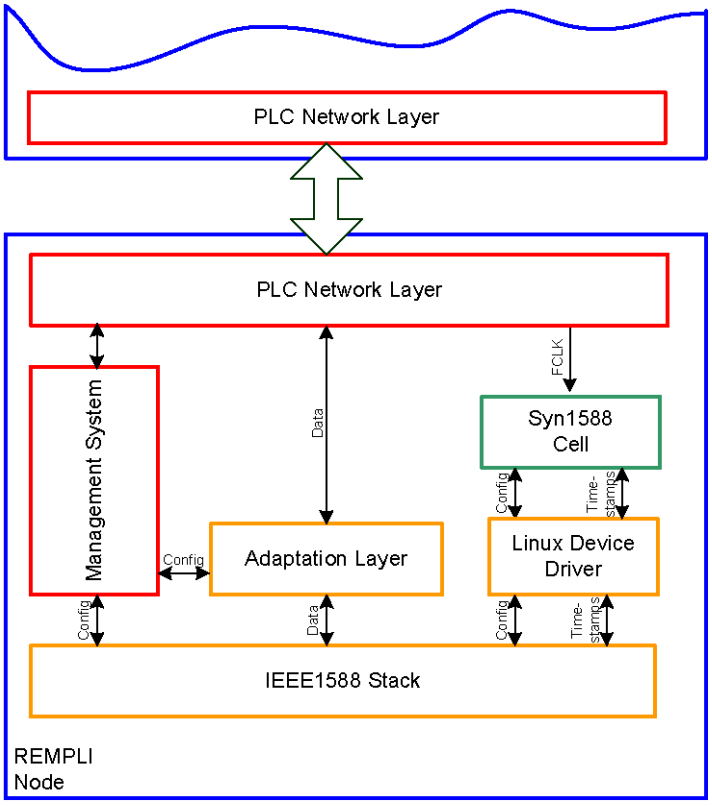

Figure 2. Integration of the adaptation layer into the REMPLI node structure.

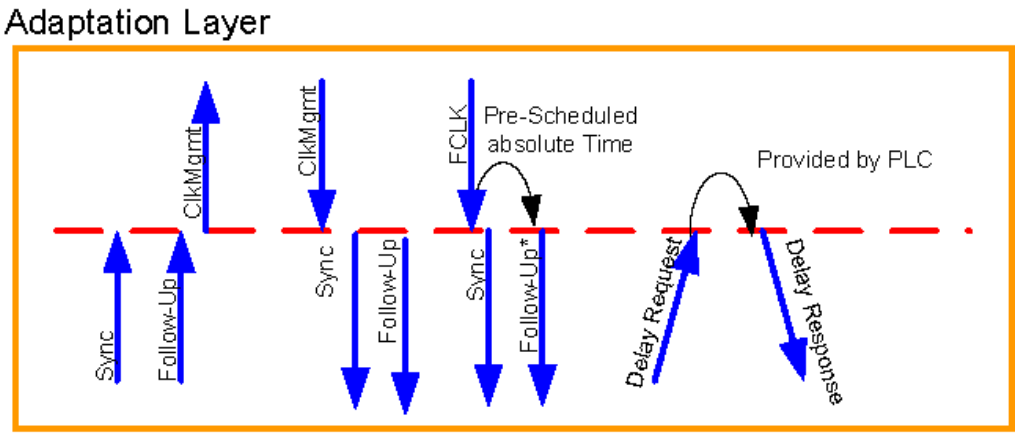

Figure 3. Detailed translation structure of the adaptation layer.

RESULTS

The preliminary results of the proposed system are evaluated in two stages:

1. Fault-tolerant *backbone network* and *access point* synchronization

2. *power line* synchronization's performance.

Theoretical results for the fault-tolerant backbone network are described in **[5]**. Moreover, using IEEE 1588 as a methodology for synchronization needs to be further evaluated, which is motivated by the enhanced hardware support used in the REMPLI project. First, as presented in **[4]**, the access point, as well as the node hardware, relies on the novel Hyperstone hyNet 32XS processor, which has a special cell supporting IEEE 1588 clock synchronization. Second, the setup itself has influence on the servo control. In the case of the investigated structure, the application for clock-synchronized nodes is the generation of pulses, with a frequency of a few kHz, which have to be coupled together with a very low phase error. In the common case, the result of those errors is a phase jitter between two nodes, which can be evaluated by means analysis of the delivered frame clock. Nevertheless, the servo design is influenced by this requirement. The clocks have to synchronize in terms of phase error as fast as possible, but may take longer to log into the absolute time of their respective master (-group).

BACKBONE NETWORK

The evaluation of the synchronization quality of the backbone network is done by using hardware support of a periodical phase-aligned hardware time interrupt. This, also called *period timer*, is compared with a period timer generated by a GPS-equipped clock. Using this phase error, the respective Allan deviation, as well as the dynamic Allan deviation, can be calculated **[6]**. Latter is defined by:

$$\sigma_y(\tau,t) = \sqrt{\frac{1}{2([T]+2)\tau^2} \sum_{i=[i]}^{i-[t+T]-2} (x_{i+2} - 2x_{i+1} + x_i)^2}. \qquad (1)$$

In that case T is the window size, defining for a one-sample-per-second evaluation. With (1), the Allan deviation can be observed as a function of time.

The stationary case is shown in Figure 4(a). A rough analysis of the curve shown in this figure suggests that the phase error is dominated by white phase noise. Further investigations using the conventional Allan deviation, as in Figure 4 (b), support this theory.

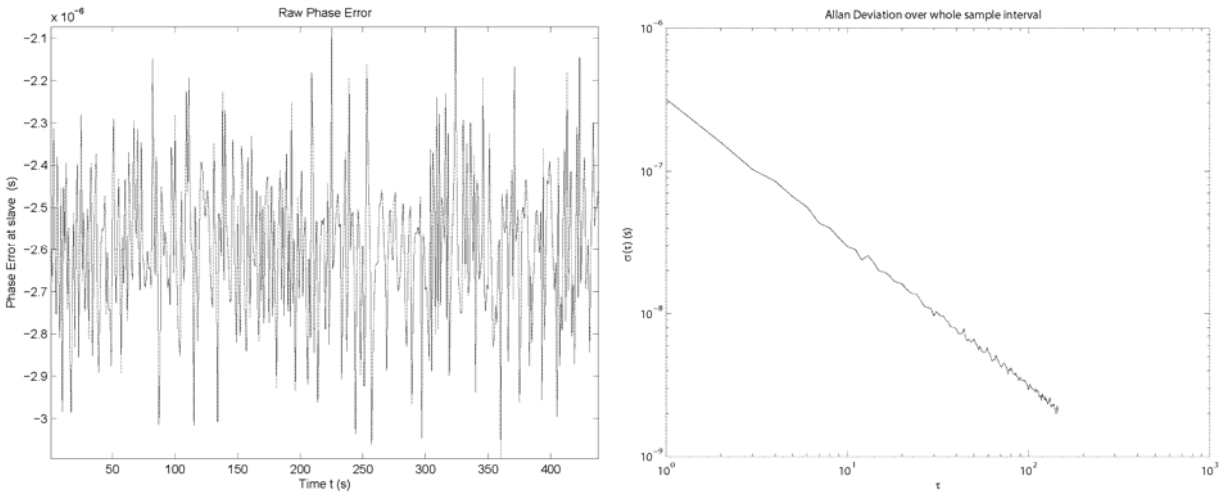

Figure 4. Phase error in the stable case and Allan deviation for the stationary case.

For a deeper investigation, also a power-up cycle as an example for a non-stationary case is evaluated. The clock quality of this experiment is shown in Figure 5. It can be seen that the quality reaches the value of the stationary case as soon as the servo has reached its stable state. The respective Allan deviation is calculated with a window size of 100 seconds. Concluding, the gained results show that, for the stationary case, the clock at an access point shows a white phase noise. Moreover, this behavior is the same of a synchronization cell-driving oscillator, which means that the phase noise is not influenced by the synchronization algorithm, but the absolute time of the clock is aligned to the one of the IEEE 1588 masters.

POWER LINE NETWORK

The presented system is at the time of this publication under investigation in a field test. Nevertheless, preliminary results from a laboratory experiment of the PLC part are presented. The test setup is constructed in such a way that the real-world parameters as dampening and noise can be modelled. Since the interface to the power line itself has no direction, dampers of 60 dB are used for emulation of the power line network. This further guarantees, on the one hand, a good communication with the neighboring PLC station and, on the other hand, no communication with the station after next. This setup is shown in Figure 6.

In this setup, one REMPLI node is configured as power line master and equipped with test software that sends synchronization packets to the power line slaves. This master unit transmits in configurable time intervals power line service telegrams (PLSTs). A telegram from a power line master reaches the slave after it is forwarded three times by the intermediate repeaters due to the relatively high dampers. Because this is just a synchronization test, no responses to the master are sent. The frame clock of the PLC master is used as external trigger event for the measurement. Each repeating node and the power line slave generate a frame clock, which is connected to a Digital Storage Oscilloscope (DSO). This allows the measurement of the jitter for each repeater level with respect to the master clock.

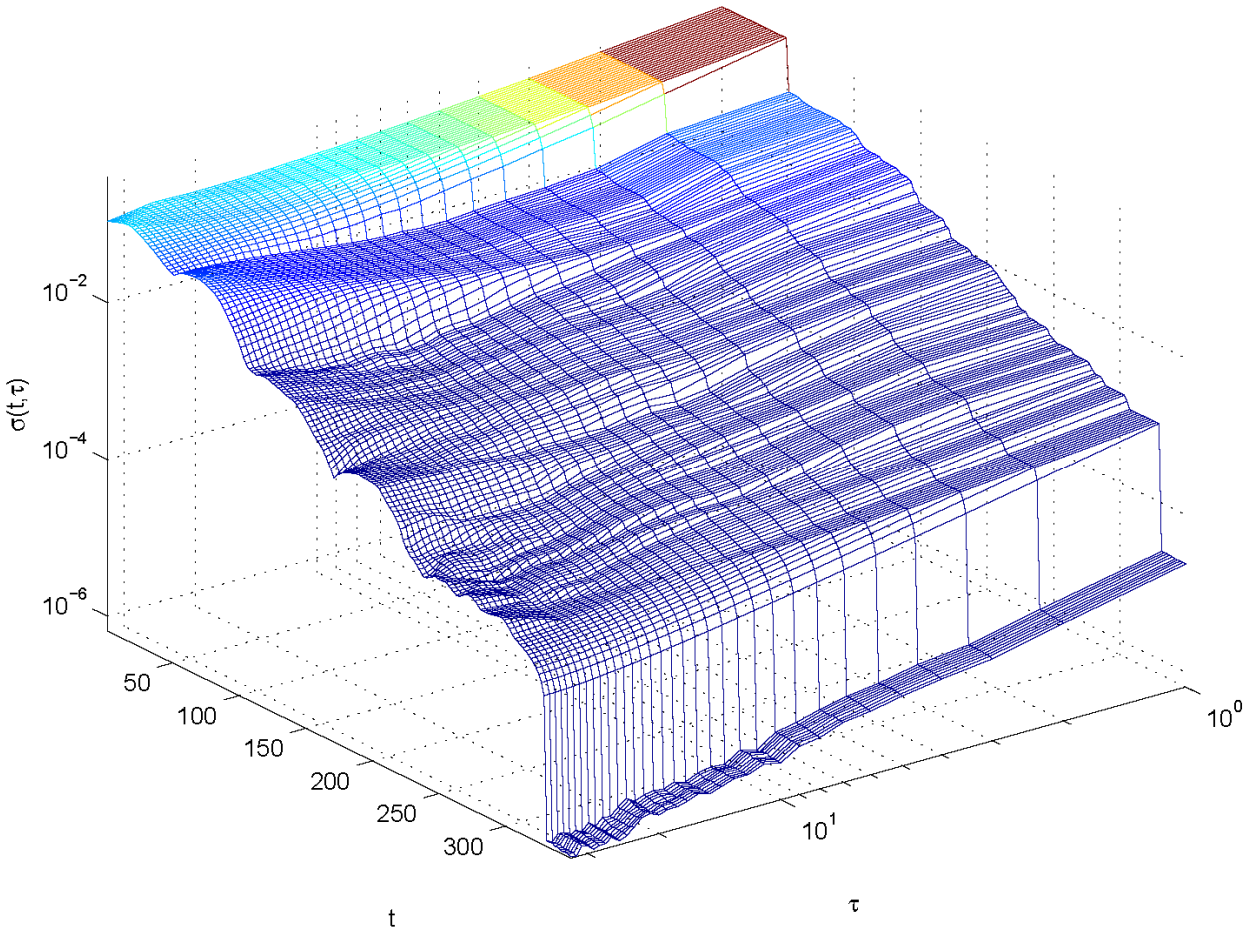

Figure5. Dynamic Allan deviation during power-up.

The measurements are shown in Table 1. In this table, the service telegram rate is varied. With a *high* PLST rate, the master transmits telegrams every 12th frame. If it is set to a *low* PLST rate, transmission is done every 505th frame. In the final system, it will not be possible to use this high rate for PLST, due to the resulting overhead in communication. Consequently, for synchronization of the frame clock every packet coming from the master will be used as an emulated IEEE 1588 packet, resulting in an effectively higher rate.

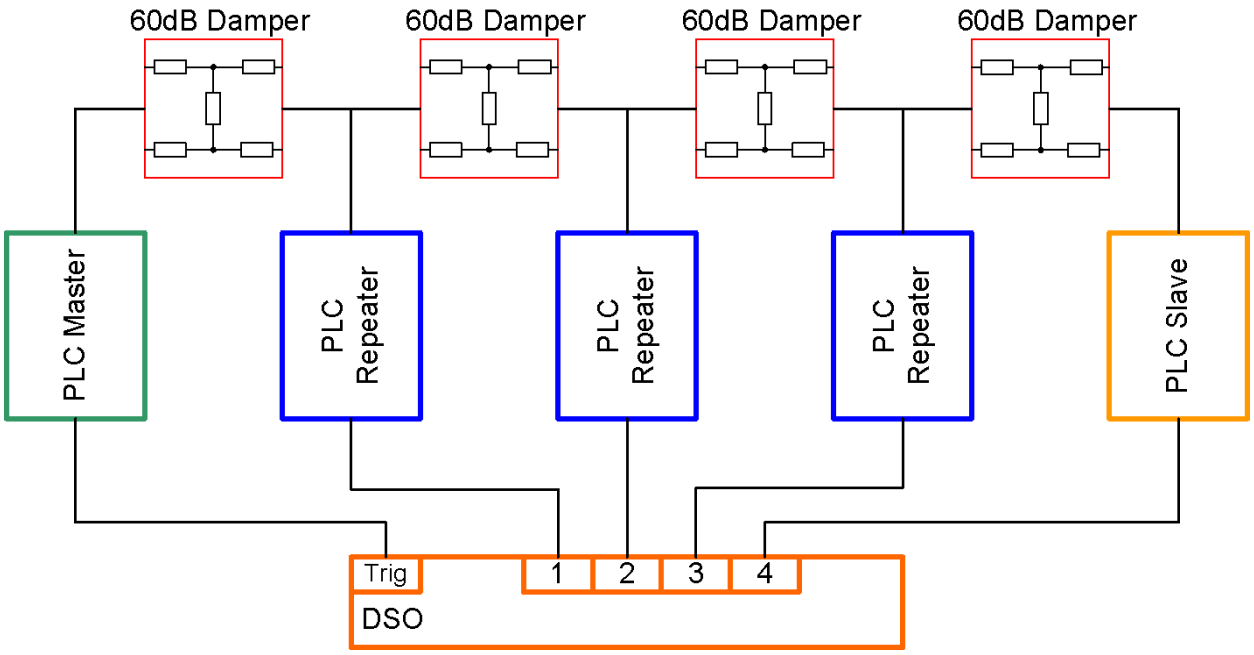

Figure 6. Test setup for PLC.

Table 1. Jitter measurements in the REMPLI PLC environment.

Band-width	PLST-rate	Jitter@Repeater level 1	2	3	4
117 kHz	low	11 µs	15 µs	31 µs	33 µs
117 kHz	high	12 µs	16 µs	21 µs	26 µs
18 kHz	low	70 µs	100 µs	121 µs	142 µs
18 kHz	high	65 µs	85 µs	105 µs	130 µs

The allowed number of repeater levels to reach the target node is limited in normal packages and consequently does not guarantee a synchronization for far end nodes. Only broadcasts like the PLST are able to reach every node in the network, even the ones which are not logged in. The special PLST can also be used during standard operation. Thus, the presented test is like a worst-case scenario for synchronization, since no other traffic is on the line. During normal operation, the situation for the lower repeater level will be more like a *high* PLST rate and only for the highest used repeater level like a low rate. Due to the better synchronization of the lower repeater levels, the jitter for the last repeater level, depending on the previous ones, will also be better.

CONCLUSION AND OUTLOOK

This paper has shown the margin conditions for clock synchronization in an environment with special needs for redundancy. This requirement for redundancy comes from the fact that a failure of a single clock synchronization master leads to instability in the connected network for the time until the next master election takes place. Consequently, the introduction of master groups in the backbone network significantly improves the overall clock quality. The loss of synchronization messages during the election of a new master is avoided, which results in the providing of steadier deviation boundaries. Furthermore, the paper shows measurements for power line communication networks, which turn out to be promising, especially in conjunction with the presented power line IEEE 1588 translation scheme. Further investigations will deal with the cascading of multiple time control loops within a heterogeneous network (Ethernet, PLC) and additional improvements to the synchronization quality concerning the algorithm used and evaluation of the currently running field test.

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